REMARKS

Applicants respectfully request favorable reconsideration of this application.

Claims 1-18 are pending.

In the Office Action, Claims 1, 6 and 10 were apparently rejected under 35 U.S.C. § 103 over Takashi in combination with Kinoshita; Claims 2, 3, 7 11 and 12 were rejected under 35 U.S.C. § 103 over Takashi and Kinoshita in further combination with Moyer; Claims 4, 5, 8, 9, 13, 14 and 15 were rejected under 35 U.S.C. § 103 over Takashi; and Claims 16-18 were rejected under 35 U.S.C. § 103 over Takashi in combination with Kinoshita and Moyer. Applicants respectfully traverse these rejections.

Independent Claims 1, 6 and 10 recite, *inter alia*, a plurality of bipolar transistors that are provided on/over a semiconductor layer that is provided over an insulation layer (e.g., an SOI device). It is apparent that Takashi does not teach or suggest such an arrangement as recited in Claims 1, 6 and 10.

For example, the portion of Takashi relied upon in the Office Action (See Office Action, page 2) is disclosed in Takashi as an "N type embedding layer 2," not an insulating layer. See, for example, Takashi, paragraph [0006]. A copy of the machine-translated detailed description of Takashi

obtained from the Japanese Patent Office website is attached hereto. It is apparent that Takashi does not teach or suggest a plurality of bipolar transistors that are provided on/over a semiconductor layer that is provided over an insulation layer as recited in Claims 1, 6 and 10.

The secondary references apparently fail to remedy the above-discussed deficiency of Takashi.

Applicants therefore respectfully request the outstanding rejections be withdrawn.

A Notice of Allowance is respectfully requested.

The Commissioner is hereby authorized to charge to Deposit Account No. 50-1165 (XA-10036) any fees under 37 C.F.R. §§ 1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this paper and has not been separately requested, such extension is hereby requested.

Respectfully submitted,

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* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the semiconductor integrated circuit which comes to dissociate two or more semiconductor devices by the component isolation region.
[0002]
[Description of the Prior Art] Drawing 5 (a) is the top view of the conventional semiconductor integrated circuit. Drawing 5 (b) is a sectional view between C-C' of drawing 5 (a). Drawing 6 is the circuit diagram of drawing 5 .
[0003] N+ mold field 13 and resistance 100-103 which are connected with the power source which is not illustrated, respectively at drawing 5 (a), The semiconductor devices 18-21 possessing the collector field 5 equipped with the base 6 and the collector contact layer 9 which have an emitter 7 and the base contact layer 8, The N type component isolation region 4-3 formed so that N+ mold field 13, and resistance 100-103 and semiconductor devices 18-21 might be touched, respectively, and the well field 12 formed in the perimeter of the N type component isolation region 4-3 are shown. In addition, the N type embedding layer 2, the P type embedding layer 3, the collector field 5, the base 6, the emitter 7, the base contact layer 8, and the collector contact layer 9 constitute semiconductor devices 18-21.
[0004] The P type embedding layer 11 prepared in the well field 12 bottom, the P type embedding layer 3 prepared in the collector field 5 bottom, the N type embedding layer 2 formed so that the P type embedding layer 3 and the N type component isolation region 4-3 might be touched, and the P type substrate 1 grounded in the gland are shown in drawing 5 (b). In addition, the collector is formed by the P type embedding layer 3 and the collector field 5.
[0005] Moreover, in drawing 5 (b), it is the parasitism PNP transistor to which the parasitism NPN transistor to which 24 supposes [the N type component isolation region 4-3] an emitter the base and the base 6 of a semiconductor device 21 for a collector and the collector field 5 of a semiconductor device 21, and 25 suppose the base and the P type substrate 1 parasitism resistance of the N type component isolation region 4-3, and 26 supposes a collector an emitter and the N type component isolation region 4-3 for resistance 10.
[0006] Moreover, the things of P type are the P type substrate 1, the P type embedding layer 3, the collector field 5, the base 6, the collector contact layer 9, resistance 10, the P type embedding layer 11, and the well field 12 among each part of drawing 5 , and although the things of N type are the N type embedding layer 2, the N type component isolation region 4, an emitter 7, the base contact layer 8, and N+ mold field 13, these conductivity types are good [things] also as reverse.
[0007] The ground line by which 44 is held in drawing 6 at touch-down potential, power-source Rhine where 45 is held at power-source potential, and 46 are a current value I0. It is the constant current source to pass. In addition, semiconductor devices 18, 19, and 21 constitute current Miller circuit, and make the semiconductor device 20 the grounded collector. Moreover, IN shows the input terminal of a semiconductor device 20, and OUT shows the output terminal of a semiconductor device 20.
[0008] It continues and actuation of the conventional semiconductor integrated circuit is explained using

drawing 6 . First, if constant current I0 flows according to a constant current source 46, since a current will flow at the base of a semiconductor device 19 based on this constant current, a current flows also to the gate of a semiconductor device 21 through the emitter of a semiconductor device 19. If a current flows to the gate of a semiconductor device 21, a current will flow a semiconductor device 21 from power-source Rhine 45 through resistance 103.

[0009] If the signal of high level is inputted at this time IN, for example, an input terminal, this current will not flow to a semiconductor device 20 side, but it will be outputted outside from an output terminal OUT. On the other hand, an output signal becomes small, in order to flow also to a semiconductor device 20 side while the current which flows a semiconductor device 21 is outputted outside from an output terminal OUT if the signal of a low level is inputted into the input terminal IN.

[0010]

[Problem(s) to be Solved by the Invention] However, since a PN junction is formed between resistance and an N type component isolation region as shown in drawing 5 (b), the conventional semiconductor integrated circuit can consider the case where this operates like parasitism diode. If parasitism diode operates, since a semiconductor integrated circuit will not operate correctly, in order to prevent this, the N type component isolation region 4-3 and the power source which is not illustrated are connected through N+ mold field 13.

[0011] If a semiconductor device 21 will be in a saturation state, parasitism NPN transistor 24 will operate, it will pass along N+ mold field 13 from power-source Rhine 45, and a current will flow at the base 6 of the semiconductor device 21 which is the emitter of parasitism NPN transistor 24. current value I0 of the current which flows according to a constant current source 46 since parasitism NPN transistor 24 is also a transistor used as a saturation state a semiconductor device 19 -- current amplification factor twice -- it is carried out and flows at the base 6 of a semiconductor device 21. By this magnification current and the parasitism resistance 25 of the N type component isolation region 4-3, a voltage drop arises in the N type component isolation region 4-3.

[0012] By this voltage drop, parasitism PNP transistor 26 will operate and a big current will flow into the P type substrate 1 from a power source. If a big current flows from a power source to the P type substrate 1, even if grand touch-down of the P type substrate 1 is carried out, the consumed electric current will increase, or a current will flow to the P type substrate 1 side through the N type component isolation region 4-1, and various problems of the potential of the P type substrate 1 rising will arise.

[0013] Then, this invention makes it a technical problem to make it the charge produced because it will be in a saturation state not influence actuation of the semiconductor device used as a saturation state.

[0014]

[Means for Solving the Problem] It is characterized by to form a separator and to come in the component isolation region which separates the semiconductor device used as the semiconductor device which this invention will divide and form the semiconductor device used as the semiconductor device which will be in a saturation state among said two or more semiconductor devices in the semiconductor integrated circuit which comes to dissociate two or more semiconductor devices by the component isolation region, and a saturation state, and will be in said saturation state, and said saturation state in order to solve the above-mentioned technical problem, so that a charge may not move mutually.

[0015] Moreover, this invention is set to the semiconductor integrated circuit which comes to dissociate two or more semiconductor devices by the component isolation region. The semiconductor device used as the semiconductor device which will be in a saturation state among said two or more semiconductor devices, and a saturation state is divided and formed. Furthermore, the inside of the semiconductor device used as said saturation state, In the component isolation region which separates the semiconductor device used as the semiconductor device it was made not to affect actuation of the semiconductor device which will not be in said saturation state when the electrical potential difference between base-emitters of the parasitic transistor which consists of the semiconductor device and component isolation region used as a saturation state is controlled, and other saturation states It is characterized by forming a separator and becoming so that a charge may not move mutually.

[0016] Furthermore, this invention is set to the semiconductor integrated circuit which comes to

dissociate two or more semiconductor devices by the component isolation region. By forming the high concentration field for considering as fixed potential near the semiconductor device which will be in a saturation state among said two or more semiconductor devices The parasitism resistance between the semiconductor devices used as this high concentration field and said saturation state is reduced, and the charge produced when the semiconductor device used as said saturation state is saturated is characterized by making it not affect actuation of other semiconductor devices.
[0017]
[Embodiment of the Invention] Hereafter, the operation gestalt of this invention is explained using a drawing.
[0018] (Operation gestalt 1) Drawing 1 (a) is the top view of the semiconductor integrated circuit of the operation gestalt 1 of this invention. Drawing 1 (b) is a sectional view between B-B' of drawing 1 (a). N+ mold field 13 and resistance 100-103 which are connected with the source of supply which supplies fixed potentials, such as a power source, to drawing 1 (a), respectively, The semiconductor devices 18-21 possessing the collector field 5 equipped with the base 6 and the collector contact layer 9 which have an emitter 7 and the base contact layer 8, The N type component isolation region 4-1 formed so that N+ mold field 13, resistance 100-103, and semiconductor devices 18-20 might be touched, respectively, The N type component isolation region 4-2 formed so that a semiconductor device 21 might be touched, and the N type component isolation region 4-1 and the well field 12 which separates 4-2 are shown.
[0019] Incidentally, semiconductor devices 18-20 will not be in a saturation state, and they explain it, assuming a semiconductor device 21 to be a thing used as a saturation state.
[0020] N+ mold field 13 and resistance 100-103, the P type embedding layer 11 prepared in the N type embedding layer 2 and 12 bottom formed under the semiconductor devices 18, 19, and 21, the P type embedding layer 3 prepared in the collector field 5 bottom, and the P type substrate 1 grounded in the gland are further shown in drawing 1 (b). In addition, the collector is formed by the P type embedding layer 3 and the collector field 5. Moreover, the separator is formed by the well field 12 and the P type embedding layer 11.
[0021] Moreover, the things of P type are the P type substrate 1, the P type embedding layer 3, the collector field 5, the base 6, the collector contact layer 9, resistance 100-103, the P type embedding layer 11, and the well field 12 among each part of drawing 1 . Although the things of N type are the N type embedding layer 2, the N type component isolation region 4-1, 4-2, an emitter 7, the base contact layer 8, and N+ mold field 13, these conductivity types are good also as reverse.
[0022] As shown in drawing 1 , with this operation gestalt, it roughly divided into semiconductor devices 18-20 and a semiconductor device 21, and formed, and the N type component isolation region 4-1 has separated the semiconductor devices 18-20, the resistance 100-103, and N+ mold field 13 used as a saturation state. Moreover, the N type component isolation region 4-2 has separated the semiconductor device 21. Furthermore, when a semiconductor device 21 is a saturation state, the well field 12 and the P type embedding layer 11 are formed so that it may not flow to the semiconductor device 18-20 side which the current produced in the PNP joint formed of the P type substrate 1, the N type component isolation region 4-2, and the collector field 5 adjoins.
[0023] In addition, although the case where the well field 12 grade was not formed in the N type component isolation region 4-1 at drawing 1 was explained to the example If the N type component isolation region 4-1 separates two or more semiconductor devices, since wiring of power-source Rhine etc. may be complicated or the area of wiring may become large It may be in the N type component isolation region 4-1 between the semiconductor devices used as a saturation state, or you may make it prepare well field 12 grade.
[0024] (Operation gestalt 2) The operation gestalt 2 of this invention explains the semiconductor integrated circuit which comes to form well field 12 grade between the semiconductor devices used as a saturation state.
[0025] Drawing 2 is the top view of the semiconductor integrated circuit of the operation gestalt 2 of this invention. In drawing 2 , 32-34 are NPN transistors ("NPN" is called hereafter.), and are equipped with the N type epitaxial field 27, the base 28, the collector contact layer 29, the base contact layer 30,

and the emitter 31, respectively.
[0026] Moreover, the N type component isolation region where 35-40 separate a semiconductor device and 4-4 separates semiconductor devices 35-38 and 40 grades, respectively, and 4-5 show the N type component isolation region for separating the collector 5 of a semiconductor device 39 with a substrate 1. In addition, it shall be a saturation state about the thing and semiconductor devices 39 and 40 which will not be in a saturation state about semiconductor devices 35-38. Incidentally, in drawing 2 , the same sign is given to the same part as drawing 1 .
[0027] Moreover, the things of P type are the base 28, the base contact layer 30, and the P type resistance 41-44 among each part of drawing 2 , and although it is the N type epitaxial field 27, the collector contact layer 29, an emitter 31, and the N type component isolation region 4-4 to 4-6, the thing of N type may be formed like the operation gestalt 1 so that these conductivity types may become reverse.
[0028] Drawing 3 is the circuit diagram of drawing 2 . As shown in drawing 3 , by NPN 32-34, semiconductor devices 35 and 39, and semiconductor devices 37 and 40, current Miller circuit is constituted, respectively and semiconductor devices 36 and 38 are made into the grounded collector. Moreover, for IN1 by which resistance 100-103 is connected between the emitter of the ******** semiconductor devices 35, 39, 37, and 40, and power-source Rhine 15, as for the output terminal of a semiconductor device 36, and IN2, the input terminal of a semiconductor device 36 and OUT1 are [the input terminal of a semiconductor device 38 and OUT2] the output terminals of a semiconductor device 38.
[0029] The base 6 of the semiconductor devices 39 and 40 saturated with this operation gestalt An emitter, The parasitism NPN transistor which uses the base and the N type component isolation region 4-4 as a collector for the collector field 5 (it is also hereafter called "Parasitism NPN".) When a current flows, even if a voltage drop arises in the N type component isolation region 4-4 by the current and parasitism resistance of the N type component isolation region 4-4 The parasitism PNP transistor which uses an emitter and the N type component isolation region 4-4 as the base, and uses the P type substrate 1 as a collector for resistance 100-103 (it is also hereafter called "Parasitism PNP".) As it did not flow, only the current which does not influence on circuit actuation prepared the well field 12 grade between the saturated semiconductor device 39 and 40, and has separated the semiconductor device 40 by semiconductor devices 35-38, the resistance 100 grade, and the N type component isolation region 4-4.
[0030] In addition, in drawing 2 , although he is trying for the N type component isolation region 4-4 to separate a semiconductor device 40, you may arrange so that the N type component isolation region 4-4 may separate a semiconductor device 39.
[0031] Below, drawing 2 and drawing 3 are used and actuation in case semiconductor devices 39 and 40 will be in a saturation state is explained. If both the electrical potential differences impressed to input terminals IN1 and IN2 rise, both the semiconductor devices 39 and 40 will be in a saturation state. When both the semiconductor devices 39 and 40 are saturated, the current based on the constant current I0 by the constant current source 16 flows to the both sides of a parasitism NPN transistor and a parasitism NPN transistor through NPN 33 and 34.
[0032] For this reason, since the current of 2I0 flows at the maximum through each parasitism NPN in N+ mold field 13, a voltage drop arises in the N type component isolation region 4-4 by this current 2I0 and parasitism resistance of the N type component isolation region 4-4. It is 2I0 temporarily. If parasitism resistance of 1mA and the N type component isolation region 4-4 is set to 400 ohms, this voltage drop will be set to 0.4V, and will become more than 0.3V. That is, the electrical potential difference between base-emitters of Parasitism PNP becomes more than 0.3V.
[0033] However, constant current I0 by the constant current source 16 If the current which flows to N+ mold field 13 by being referred to as 500microA is made into one half, a voltage drop will be set to 0.2V and will not exceed 0.3V. Thus, if it is made for the electrical potential difference between base-emitters of Parasitism PNP not to exceed 0.3V, as shown in drawing 2 , it will also become possible to form a semiconductor device 40 in a semiconductor device 35-38 side.
[0034] Here, the basis of the voltage drop of the N type component isolation region 4-4 considering as

less than [0.3V] is explained. Ie is [Equation 1] when the emitter current of a bipolar transistor is set to Ie.

$$I_e \approx I_s \exp\left(\frac{q}{kT} V_{BE}\right) \cdots (1)$$

1.3806x10-23 [J/K] and q can be expressed in the amount of electronic charge as 1.6022x10-19 [C], and VBE can express the emitter current and k whose (Ie is a bipolar transistor as electrical-potential-difference between base-emitters) in a Boltzmann's constant. Moreover, [Equation 2]

$$I_s = f * T^{4-a} \exp\left(\frac{-qE_g}{kT}\right) \cdots (2)$$

(f can express a constant, a**2, and Eg in the energy gap of silicon as 1.12[V]).

[0035] Here, in ordinary temperature (T= 27 degrees C), it is kT/q**26mV, and generally, since it is about Is =1x10-15 then, if these are substituted for a formula 1, it will be set to Ie **0.1nA at the time of VBE=0.3V.

[0036] Next, if it asks for a constant f**0.057 and considering a hot condition the case of T=400K (127 degrees C) is calculated from a formula 2 using general Is =1x10-15 (atT=27 degree C), it will be set to Is **4.5x10-11 from a formula 2. When VBE is 0.3V (atT=400K), it is kT/q**34mV (atT=400K), and it will be set to Ie **0.3microA if these are substituted for a formula 1. Therefore, for the circuit where a current micro[dozens of] A-micro[hundreds of] A Flows, if VBE is less than [0.3V], even if it will take a temperature change etc. into consideration, it is Ie. It is very small.

[0037] However, if Is**4.5x10-11, kT/q**34mV, and VBE=0.5V are substituted for a formula 1 like the above-mentioned when VBE is 0.5V (atT=400K) at an elevated temperature, it will be set to Ie **110microA, and the effect of a current which flows to Parasitism PNP will become large for the circuit where a current micro[dozens of] A-micro[hundreds of] A Flows.

[0038] That is, if it is made for the electrical potential difference between base-emitters of Parasitism PNP not to exceed 0.3V, even if it considers the temperature characteristic for Parasitism PNP, generally only a very small current which does not influence other semiconductor devices will flow.

[0039] Moreover, although the example in case two semiconductor devices 39 and 40 will be in a saturation state here was shown If it is made to become less than [0.3V], the voltage drop of the N type component isolation region 4-6 produced by the current which flows to Parasitism NPN when these semiconductor devices will be in a saturation state, and parasitism resistance of the N type component isolation region 4-6 Even if it is the case where three or more semiconductor devices will be in a saturation state, the location which forms well field 12 grade can be made into between the semiconductor devices used as a saturation state.

[0040] In addition, if the N type component isolation region 4-1 separates two or more semiconductor devices, since wiring of power-source Rhine etc. may be complicated or the area of wiring may become large like the operation gestalt 1, it may be in the N type component isolation region 4-1 between the semiconductor devices used as a saturation state, or you may make it prepare well field 12 grade.

[0041] (Operation gestalt 3) Drawing 4 is the top view of the semiconductor integrated circuit of the operation gestalt 3 of this invention. In addition, drawing 4 is arranged based on the circuit diagram shown in drawing 3 . In drawing 4 , 4-6 is an N type component isolation region for separating a semiconductor device 35 - 40 grades, respectively. Moreover, even if it is the case where parasitism resistance of the N type component isolation region 4-6 will be reduced, and semiconductor devices 39 and 40 will be in a saturation state, respectively, by arranging N+ mold field 13 near the semiconductor devices 39 and 40 unlike drawing 2 , he is trying only for the current which does not influence on circuit actuation not to flow for Parasitism PNP in drawing 4 . In addition, in drawing 4 , the same sign is given to the same part as drawing 2 .

[0042] With this operation gestalt, as about 1/is set to 10 as compared with the case of the operation gestalt 2 in distance with the semiconductor devices 39 and 40 used as N+ mold field 13 and a saturation state, about 1/of parasitism resistance of the N type component isolation region 4-6 is set to 10. Therefore, even if a current 2I0 flows from a power source to the P type substrate 1, the voltage drop of the N type component isolation region 4-6 is small, for example, since it does not become more than 0.3V, only the current which does not influence on circuit actuation flows for Parasitism PNP. In such a case, even if it has the semiconductor devices 39 and 40 used as a saturation state, a semiconductor integrated circuit can be constituted, without forming well field 12 grade between semiconductor devices 35-40.

[0043] In addition, although the example in case two semiconductor devices 39 and 40 will be in a saturation state here was shown If it is made to become less than [0.3V], the voltage drop of the N type component isolation region 4-6 produced by the current which flows to Parasitism NPN when these semiconductor devices will be in a saturation state, and parasitism resistance of the N type component isolation region 4-6 Even if it is the case where three or more semiconductor devices will be in a saturation state, it can avoid well field 12 grade separating each semiconductor device.

[0044] Moreover, if the N type component isolation region 4-1 separates two or more semiconductor devices, since wiring of power-source Rhine etc. may be complicated or the area of wiring may become large like the operation gestalt 1, it may be in the N type component isolation region 4-1 between the semiconductor devices used as a saturation state, or you may make it prepare well field 12 grade.

[0045] Furthermore, although it explained that the current which flows to Parasitism PNP did not have effect on circuit actuation with the operation gestalten 2 and 3 when the N type component isolation region 4-4 and the voltage drop of 4-6 were or less about 0.3V, respectively What is necessary is just to restrict so that the voltage drop of the N type component isolation region 4-1 may turn into less than [0.5V] if it seems that the current which flows to Parasitism PNP does not influence on circuit actuation even if it is an electrical potential difference beyond 0.3V so that the N type component isolation region 4-4 and the voltage drop of 4-6 may be 0.5V.

[0046]

[Effect of the Invention] Since the semiconductor device used as the semiconductor device used as a saturation state and a saturation state is separated according to this invention as explained above, the charge produced because it will be in a saturation state can be prevented from influencing actuation of the semiconductor device used as a saturation state.

[0047] Moreover, since this invention separates the semiconductor device used as the semiconductor device it was made not affect actuation of the semiconductor device used as a saturation state, and other saturation states when the electrical potential difference between base-emitters of the parasitic transistor which consists of the semiconductor device and the component isolation region which will be in a saturation state among the semiconductor devices used as a saturation state is controlled, it can prevent from influencing actuation of the semiconductor device from which the charge produced because it will be in a saturation state will not be in a saturation state.

[0048] Furthermore, since this invention is reducing the parasitism resistance between the semiconductor devices which will be in a high concentration field and a saturation state by forming the high concentration field for considering as fixed potential near the semiconductor device used as a saturation state, it can be prevented from influencing actuation of the semiconductor device from which the charge produced because it will be in a saturation state will not be in a saturation state.

[Translation done.]